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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application of

Applicant	:	Howard E. Rhodes and Luan Tran
Serial No	:	09/008,531
Filed	:	January 16, 1998
Title	:	**METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING IMPROVED CONTACTS**
Docket	:	MIO 0012 V2 (94-0012.04)
Examiner	:	M. Trinh
Art Unit	:	2822
Conf. No	:	6336

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 1, 2006.

Susan M. Luna
Agent **Reg. No. 38,769**

Sir:

BRIEF ON APPEAL

This is an appeal from the Office Action mailed October 5, 2005, finally rejecting claims 21-25, 31, and 32, all of the claims in the application. A Notice of Appeal was timely mailed on January 5, 2006, with the accompanying fee. Our check in the amount of $500 accompanies this Brief in accordance with 37 CFR §41.20(b)(2).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office.

Related Appeals and Interferences

Applicant knows of no currently pending related appeals or interferences that would have an effect on the outcome of this appeal. This application was the subject of a prior appeal, but no decision was rendered by the Board. See the Office Action mailed April 6, 2005.

Status of Claims

Claims 21-25, 31, and 32 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

All of the amendments previously filed in this application have been entered.

Summary of Claimed Subject Matter

Applicants' invention is directed to a method of making a semiconductor device and in one embodiment includes forming a conductive layer having a topography that includes a substantially vertical component, forming an overlayer, etching a contact hole in the overlayer in an overetch amount into the substantially vertical component of the conductive layer, and forming a contact in the hole adjacent to and directly contacting the vertical component of the conductive layer.

As described in the specification at pages 2-3 and shown in Figs. 1, 2, 3A, and 3B, with prior art fabrication techniques, it was difficult to ensure that contact holes etched through an overlayer would stop precisely on the conductive layer to which the contact would be made. For example, as described at page 3, lines 17-34, and shown in Figs. 3A and 3B, a contact hole can be overetched into and sometimes through cell poly layer 2. Such a result diminishes the effectiveness of the contact by causing undesirable high resistance between conductor 16 and cell poly 2 (Fig. 3A) or may even cause electrical shorting (Fig. 3B).

In an embodiment of the present invention described at pages 8-11 and shown in Figs. 4-7, a substrate 22, 23, having at least one semiconductor layer is provided. An underlayer 20 having an opening 24 is formed over the semiconductor layer (page 8, lines 8-20). A layer of conductive material 26 is formed over the underlayer and into the opening (Fig. 5), the conductive material having a topography that includes a substantially vertical component in the opening which is defined by a localized thick region in the layer of conductive material. An overlayer 28 is then formed over the layer

of conductive material. As shown in Fig. 5, the thickness of the overlayer 28 is greater than the thickness of the underlayer 20.

Referring to Fig. 6, and page 8, lines 21-32, a contact hole 30 is etched in the overlayer and in an overetch amount which extends into, but not through the substantially vertical component of the layer of conductive material in the opening. As shown in Fig. 7, and described at page 9, lines 29-34 and page 10, lines 1-2, a contact 32 is then formed in the contact hole which is disposed adjacent to and directly contacting the vertical component of the conductive material.

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection for review on appeal are:

(1) Claims 31-32 are rejected under 35 USC §112, second paragraph, as being indefinite.

(2) Claims 21-23 and 25 stand rejected under 35 USC §102(e) as being anticipated by Jost et al. (US 5,563,089).

(3) Claims 21-25 and 31-32 stand rejected under 35 USC §102(e) as being anticipated by Jun (US 5,459,094).

(4) Claims 21-22, 24, and 31-32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont (US 5,484,741) taken with Toshiyuki et al. (JP-05-109905) and Zamanian (US 5,793,111).

Grouping of Claims

The Examiner has stated four grounds of rejection, rejecting claims 31-32 under 35 USC §112, second paragraph, as being indefinite; rejecting claims 21-23 and 25 under 35 USC §102(e) as being anticipated by Jost et al. (US 5,563,089); rejecting claims 21-25 and 31-32 under 35 USC §102(e) as being anticipated by Jun (US 5,459,094); and rejecting claims 21-22, 24, and 31-32 as being unpatentable over Bergemont (US 5,484,741) taken with Toshiyuki et al. (JP-05-109905) and Zamanian (US 5,793,111).

This application contains two independent claims, claims 21 and 31. Applicants will separately argue the patentability of those claims and additional dependent claims in the body of their argument section.

Argument

Rejection under 35 U.S.C. 112, second paragraph

In the final Office Action mailed October 5, 2005, the Examiner pointed out that there is insufficient antecedent basis for the limitation "said overlayer having a thickness greater than ***said underlayer***" as recited in claim 31. Applicants submit that, given the opportunity, they will amend claim 31 to provide proper antecedent basis for the term "underlayer" so that claims 31 and 32 are in compliance with 35 U.S.C. 112, second paragraph.

Rejection under 35 U.S.C. 102(e) as being anticipated by Jost et al. (U.S. 5,563,089).

Claim 21

Claim 21 recites, inter alia, a process for making a semiconductor device comprising the steps of providing a substrate having at least one semiconductor layer, forming an underlayer having an opening over the semiconductor layer; forming a layer of conductive material over the underlayer which has a topography that includes a substantial vertical component in the opening, forming an overlayer over the layer of conductive material, where the overlayer has a thickness greater than the underlayer, etching a contact hole in the overlayer in an overetch amount into but not through the substantially vertical component of the layer of conductive material in the opening, and forming a contact in the contact hole disposed adjacent to and directly contacting the vertical component.

Jost et al. teach a method of forming a bit line construction in which an array of word lines 12, 14, 16 are placed on a semiconductor substrate 11, an electrically insulating material 28 is placed over the word lines, contact openings 32, 34 are provided

through the insulating layer, a first layer of an electrically conductive material 36 is placed over the insulating layer, a capacitor dielectric layer 38 is placed over the first conductive layer, a second layer 40 of conductive material is provided in the contact openings, a bit line insulating layer 44 is placed over the second conductive material, and a bit contact opening is patterned through the bit line insulating layer 44a.

The Examiner asserts that Jost et al.'s method includes providing a semiconductor substrate 11, forming an "underlayer" 20, 28 having an opening over the semiconductor layer, forming a conductive layer 40 over the underlayer which includes a substantially vertical component in the opening of the underlayer, forming an "overlayer" 44a over the conductive layer 40, and etching a contact hole in the overlayer 44a in an overetch amount into but not through the vertical component of layer 40.

However, Jost et al. do not teach etching **into**, but not through, the substantially vertical component of the conductive layer as recited in claim 21. While Jost et al. teach an overetch into the conductive layer 40, it is noted that this overetch does not extend **into** the **vertical component** of their conductive layer, i.e., the substantially vertical component of layer 40 in the opening formed over the semiconductor layer. Rather, Jost et al. show that the etching of layer 44a extends only into the upper surface of conductive layer 40, not into the vertical component of the layer. See Fig. 11. As required by applicants' claims, the overetch amount is etched "*into* but not through the substantially **vertical component** of said layer of conductive material." See also applicants' Fig. 7 where it can be clearly seen that the overetch extends into the vertical component (localized thick region 34) of the conductive layer 26.

The Examiner appears to have misinterpreted this limitation of applicants' previously amended claims as he stated in the final rejection that Jost et al. do not overetch in an amount which extends "through the substantially vertical component" and that "substantial vertical components of the conductive layer 40 is remained in the opening after etching." This does not meet applicants' claims. Applicants' claim 21 requires *both* that the etching extend **into** the vertical component *and* that it does not extend entirely **through** the vertical component.

As Jost et al. do not teach a method of etching into the vertical component of their conductive layer, they cannot anticipate claim 21.

Claim 22

With regard to claim 22, which recites that the vertical component defines a localized thick region in the layer of conductive material, again it is clear that Jost et al. do not teach or suggest etching into the vertical component of the layer which contains a localized thick region as claimed, but rather Jost et al. etch into a surface portion of their conductive material. See Fig. 11 of Jost et al. Claim 22 is believed to be patentable over Jost et al. for the same reasons discussed above with regard to claim 21.

Claim 23

Claim 23, which recites that the vertical component is a spacer, is also believed to be patentable over Jost et al., who do not teach or suggest a vertical component of their conductive material as a spacer. The only spacer structures shown by Jost et al. are spacers 18 and 51.

Claim 25

Claim 25 recites that the conductive layer is a capacitor electrode, applicants submit that there is no teaching or suggestion in Jost et al. that their conductive layer 40 would function as a capacitor electrode. Rather, layer 40 forms an electrically conductive annular ring positioned in a bit line plug. Claim 25 is also believed to be patentable for the same reasons discussed above with regard to claim 21.

Rejection under 35 U.S.C. 102(e) as being anticipated by Jun (U.S. 5,459,094).

Claim 21

Jun teaches a method for making a semiconductor memory device. Referring to Figs. 4a-4f, Jun teaches a film oxide 11 and a gate oxide film 12 formed on a semiconductor substrate 100. A first insulating film 14 is formed over the entire structure

and is etched to form a contact hole 15. A conductive layer 16 is formed over the insulating film 14 and a second insulating layer 17 is formed over the first conductive layer. A photoresist film is coated over the second insulating layer 17. The second insulating layer 17 and the conductive layer 16 are then etched. A second conductive layer 19 is then formed over the structure and is etched to expose insulating layer 17.

The Examiner refers to Figs. 4a-4f and 8a-8f of Jun, asserting that Jun teaches a substrate 100 having a semiconductor layer, forming a gate insulating layer ("underlayer") 12 having an opening 15 over the semiconductor layer, forming a conductive layer 16 over the "underlayer" which has a substantially vertical component, forming an insulating "overlayer" 17 over the conductive layer 16, etching a contact hole in the "overlayer" in an overetch amount into but not through the vertical component of layer 16, and forming a contact 19 in the contact hole.

As interpreted by the Examiner, Jun teaches an "underlayer" 12 and an "overlayer" 17. However, applicants wish to point out that Jun teaches no layer of conductive material formed over the "underlayer" 12 as required in claim 21. Rather, conductive layer 16 is formed over insulating layer 14. Assuming that insulating layer 14 could be interpreted as an "underlayer," applicants wish to point out that insulating layer 14 is clearly greater in thickness than "overlayer" 17. See Fig. 4b. As recited in claim 21, the overlayer must have a thickness **greater** than the underlayer, not the other way around as taught in Jun.

Applicants further wish to point out that Jun does not teach etching a contact hole in the overlayer in an overetch amount **into**, but not through the substantially vertical component of the conductive layer as claimed. While Jun et al. teach etching into the surface of conductive layer 16, this etching does not extend **into** the substantially **vertical component** of the conductive layer. See Fig. 4c. Claim 21 is patentable over Jun.

Claim 22

As discussed above, Jun do not teach or suggest etching into the vertical portion of the layer which defines a localized thick region in the conductive layer as claimed. Rather, Jun etch into the surface portion of their conductive material 16. Claim 22 is

believed to be patentable over Jun for the same reasons discussed above with regard to claim 21.

Claim 23

Claim 23 is also believed to be patentable over Jun as Jun does not teach or suggest that the substantially vertical component of their conductive layer 16 can function as a spacer.

Claim 24

Claim 24 is believed to be patentable for the same reasons discussed above with regard to claim 21.

Claim 25

Claim 25 is believed to be patentable for the same reasons discussed above with regard to claim 21.

Claim 31

Applicants submit that claim 31 is patentable for the same reasons presented above with regard to claim 21; i.e., Jun does not teach or suggest a process in which a contact hole extends **into** the **vertical component** of the layer of conductive material as claimed.

Claim 32

As discussed above, Jun do not teach or suggest etching into the vertical component of the layer which defines a localized thick region in the conductive layer as claimed.

Rejection under 35 U.S.C. 103(a) as being unpatentable over Bergemont (5,484,741) taken with Toshiyuki et al. (JP 05-109905) and Zamanian (5,793,111).

Claim 21

Bergemont teaches a method of forming a flash EPROM array. The Examiner refers to Figs. 9-14 of Bergemont, asserting that Bergemont teach a method for forming a semiconductor device which includes providing a semiconductor substrate 102, forming an "underlayer" 118 over the semiconductor layer, forming a layer of conductive material 122 over the underlayer 118 including a substantially vertical component, forming an "overlayer" 124 over the layer of conductive material, etching a contact hole in the overlayer 124 to expose the substantially vertical component of the conductive material 122, and forming a contact 126 in the contact hole.

In the final rejection, the Examiner acknowledges that Bergemont does not teach etching in an overetch amount into, but not through the substantially vertical component of layer 122 as recited in the claims, but asserts that Toshiyuki et al. (JP 05-109905) teaches forming a layer of conductive material 2 over an "underlayer," forming an "overlayer" 3 over the layer of conductive material, etching to forming a contact hole 9 in the overlayer 3 and in an overetch amount into but not through the layer of the conductive material having a vertical component.

The Examiner further asserts that Zamanian teaches etching a contact hole in an "overlayer" 40 in an overetch amount into, but not through a layer of conductive material having a substantially vertical component. The Examiner has taken the position that it would have been obvious to etch a contact hole in the "overlayer" 124 of Bergemont in an overetch amount into but not through the layer 122 in view of Toshiyuki and Zamanian.

Applicants submit that neither Toshiyuki nor Zamanian teach etching **into**, but not through the substantially **vertical component** of a conductive layer as claimed. As discussed above and as shown in Figs. 6 and 7, applicants' layer of conductive material 26 includes a substantially vertical component 34. Toshiyuki does not teach or suggest a layer of conductive material having such a substantially vertical component. Rather,

conductive layer 2 is formed as a horizontal layer having no substantially vertical component as defined in the present invention. See the Abstract of Toshiyuki which teaches that the bottom plane of layer 2 is almost flat. As conductive layer 2 has no substantially vertical component, Toshiyuki cannot teach etching into, but not through a substantially vertical component of a conductive layer as claimed.

Zamanian teaches a semiconductor integrated circuit having an improved landing pad which includes an oxide layer 28 with a contact opening 30, a polysilicon layer 32 formed over the oxide layer 28 and opening 30, a silicide layer 36 formed over the polysilicon layer 32, and a barrier layer formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are also formed. Assuming that the Examiner is referring to polysilicon layer 32 as the "conductive layer" underlying "overlayer" 40, there is no teaching in Zamanian that the vertical component of this layer is etched as claimed. See Fig. 6 of Zamanian.

Again, the Examiner appears to have misinterpreted the limitation of applicants' claims in his statements that the references teach an overetch amount "into but not through the layer of **conductive material** having a substantially vertical component." See the final rejection at page 6. This is not a proper interpretation of applicants' claims, which recite that the overetch amount extends "into, but not through the **substantially vertical component** of the layer of conductive material," *not* into any portion of the conductive material. As the none of the cited references teach or suggest overetching in an amount which extends into the substantially vertical component of the conductive layer, they do not render the claims obvious.

Nor is there any motivation to combine the teachings of the references. Each of the cited references solve a different problem and show different geometries for their structures. The Examiner has failed to carry his evidentiary burden of demonstrating where in the prior art the suggestion or motivation for modifying these reference teachings can be found.

Claim 22

As discussed above, none of the cited references teach or suggest etching into the vertical component which is defined by a localized thick region in the conductive layer as claimed. Claim 22 is believed to be patentable over Bergemont, Toshiyuki and Zamanian for the same reasons discussed above with regard to claim 21.

Claim 24

Claim 24 is believed to patentable for the same reasons discussed above with regard to claim 21.

Claim 31

Applicants submit that claim 31 is patentable for the same reasons presented above with regard to claim 21; i.e., the cited references do not teach or suggest a process in which a contact hole extends **into** the substantially **vertical component** of the layer of conductive material as claimed.

Claim 32

Claim 32 is believed to be patentable for the same reasons discussed above with regard to claim 22.

Conclusion

The claims are not anticipated by Jost et al. or Jun, neither of which teach overetching into, but not through a substantially vertical component of a conductive layer in a semiconductor device. In addition, the Examiner has failed to carry his evidentiary burden of establishing a prima facie case of obviousness with respect to all of the claims

on appeal. The Board is requested to reverse all of the prior art rejections made by the Examiner in their entirety. Applicants stand read to amend claim 31 to overcome the indefiniteness problem.

Respectfully submitted,

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SML/

CLAIMS APPENDIX

21. A process for making a semiconductor device comprising the steps of:

providing a substrate having at least one semiconductor layer;

forming an underlayer having an opening over the at least one semiconductor layer;

forming a layer of conductive material over the underlayer and in said opening, said layer of conductive material having a topography that includes a substantially vertical component in said opening;

forming an overlayer over the said layer of conductive material said overlayer having a thickness greater than said underlayer;

etching a contact hole in said overlayer and in an overetch amount into but not through the substantially vertical component of said layer of conductive material in said opening; and

forming a contact in said contact hole disposed adjacent to and directly contacting said vertical component.

22. A process as claimed in claim 21 wherein said vertical component defines a localized thick region in the layer of conductive material.

23. A process as claimed in claim 21 wherein said vertical component is a spacer.

24. A process as claimed in claim 21 further comprising the step of forming a structure having an opening therein under said conductive layer and filling said opening with said conductive material to form said vertical component.

25. A process as claimed in claim 21 wherein said conductive layer is a capacitor electrode.

31. A process for making a semiconductor device comprising:

providing a substrate having at least one semiconductor layer;

forming a structure having an opening in said at least one semiconductor layer;

forming a layer of conductive material over said at least one semiconductor layer;

filling said opening with said conductive material to form a substantially vertical component in said opening;

forming an overlayer over said layer of conductive material, said overlayer having a thickness greater than said underlayer;

forming a contact hole in said overlayer and extending into said vertical component of said layer of conductive material, said contact hole disposed adjacent to and directly contacting said vertical component in said opening; and

filling said contact hole with a conducting material.

32. A process as claimed in claim 31 wherein said vertical component defines a localized thick region in the layer of conductive material.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/008,531
Filing Date	January 16, 1998
First Named Inventor	Howard E. Rhodes
Examiner Name	M. Trinh
Art Unit	2822
Attorney Docket No.	MIO 0012 V3 (94-0012.04)

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Brief On Appeal	500.00

SUBMITTED BY

Signature	Susan M. Luna	Registration No. (Attorney/Agent) 38,769	Telephone (937) 449-6400
Name (Print/Type)	Susan M. Luna - Agent		Date March 1, 2006